FIG. 1

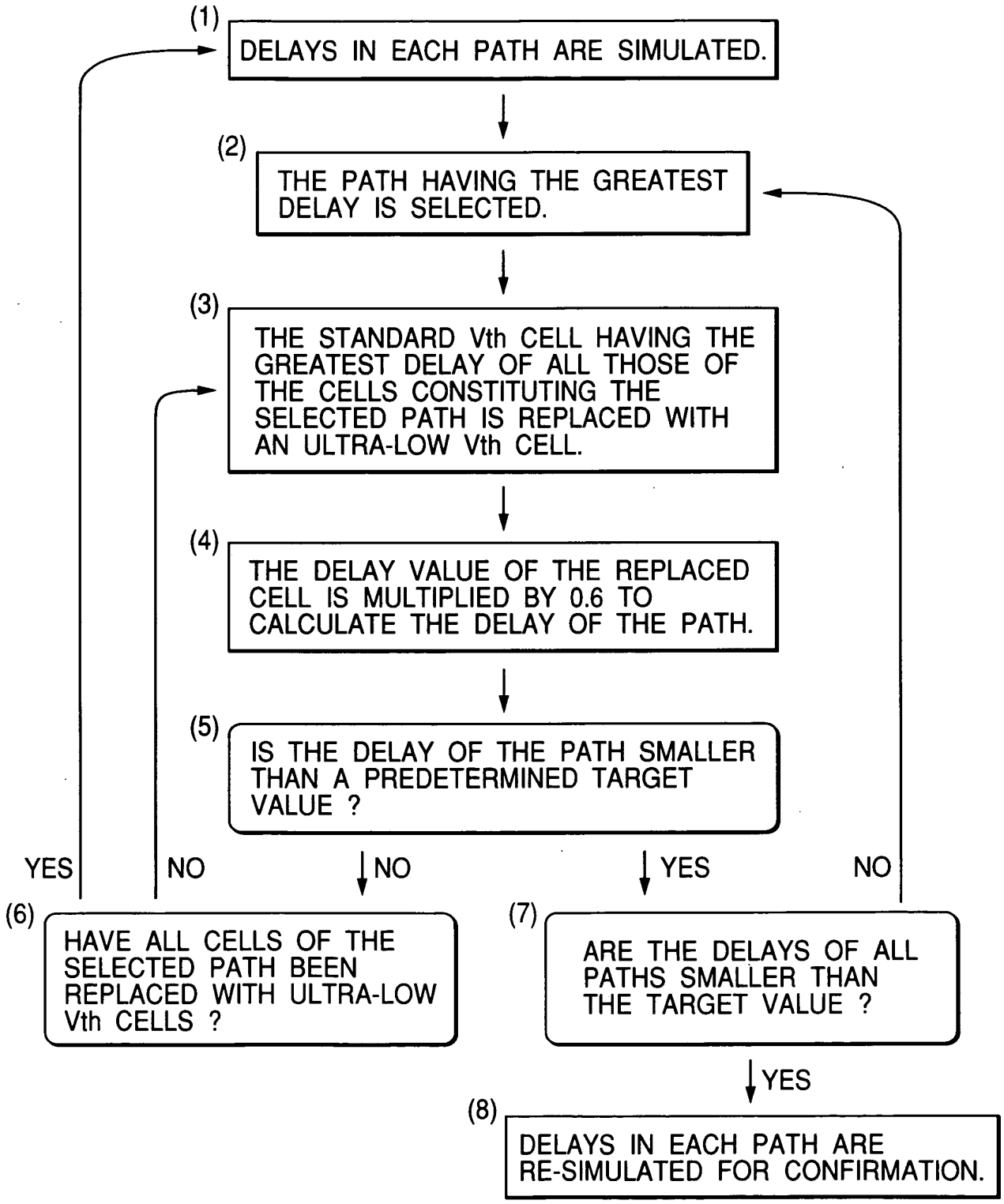
(1)
DELAYS IN EACH PATH ARE SIMULATED.
(2)
THE PATH HAVING THE GREATEST DELAY IS SELECTED.
(3)
THE STANDARD Vth CELL HAVING THE GREATEST DELAY OF ALL THOSE OF THE CELLS CONSTITUTING THE SELECTED PATH IS REPLACED WITH AN ULTRA-LOW Vth CELL.
(4)
THE DELAY VALUE OF THE REPLACED CELL IS MULTIPLIED BY 0.6 TO CALCULATE THE DELAY OF THE PATH.
(5)
IS THE DELAY OF THE PATH SMALLER THAN A PREDETERMINED TARGET VALUE ?
YES
NO
NO
YES
NO
(6)
HAVE ALL CELLS OF THE SELECTED PATH BEEN REPLACED WITH ULTRA-LOW Vth CELLS ?
(7)
ARE THE DELAYS OF ALL PATHS SMALLER THAN THE TARGET VALUE ?
YES
(8)
DELAYS IN EACH PATH ARE RE-SIMULATED FOR CONFIRMATION.

FIG. 2

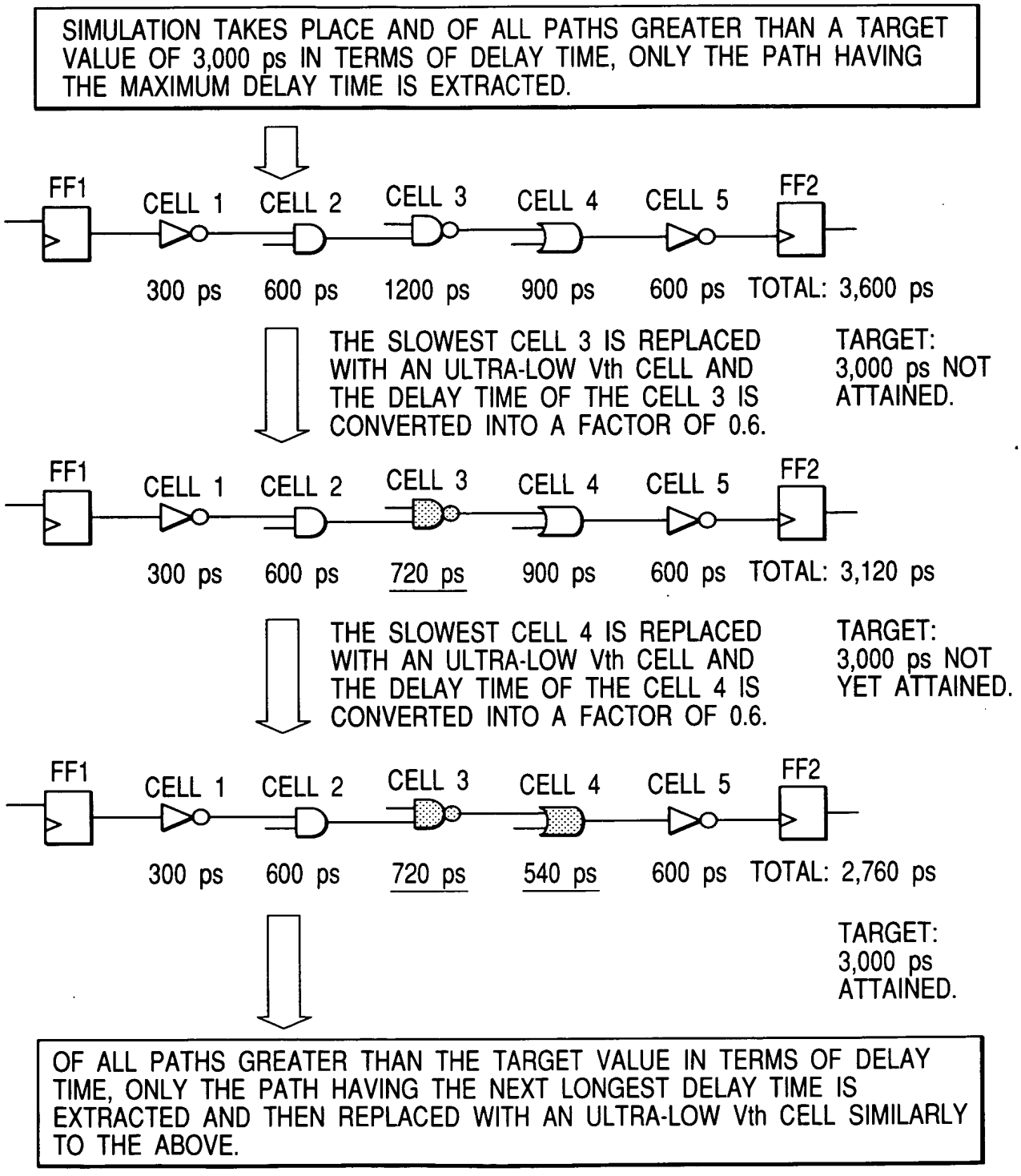
SIMULATION TAKES PLACE AND OF ALL PATHS GREATER THAN A TARGET VALUE OF 3,000 ps IN TERMS OF DELAY TIME, ONLY THE PATH HAVING THE MAXIMUM DELAY TIME IS EXTRACTED.
FF1
CELL 1
CELL 2
CELL 3
CELL 4
CELL 5
FF2
300 ps
600 ps
1200 ps
900 ps
600 ps
TOTAL: 3,600 ps
THE SLOWEST CELL 3 IS REPLACED WITH AN ULTRA-LOW Vth CELL AND THE DELAY TIME OF THE CELL 3 IS CONVERTED INTO A FACTOR OF 0.6.
TARGET: 3,000 ps NOT ATTAINED.
FF1
CELL 1
CELL 2
CELL 3
CELL 4
CELL 5
FF2
300 ps
600 ps
720 ps
900 ps
600 ps
TOTAL: 3,120 ps
THE SLOWEST CELL 4 IS REPLACED WITH AN ULTRA-LOW Vth CELL AND THE DELAY TIME OF THE CELL 4 IS CONVERTED INTO A FACTOR OF 0.6.
TARGET: 3,000 ps NOT YET ATTAINED.
FF1
CELL 1
CELL 2
CELL 3
CELL 4
CELL 5
FF2
300 ps
600 ps
720 ps
540 ps
600 ps
TOTAL: 2,760 ps
TARGET: 3,000 ps ATTAINED.
OF ALL PATHS GREATER THAN THE TARGET VALUE IN TERMS OF DELAY TIME, ONLY THE PATH HAVING THE NEXT LONGEST DELAY TIME IS EXTRACTED AND THEN REPLACED WITH AN ULTRA-LOW Vth CELL SIMILARLY TO THE ABOVE.

FIG. 3

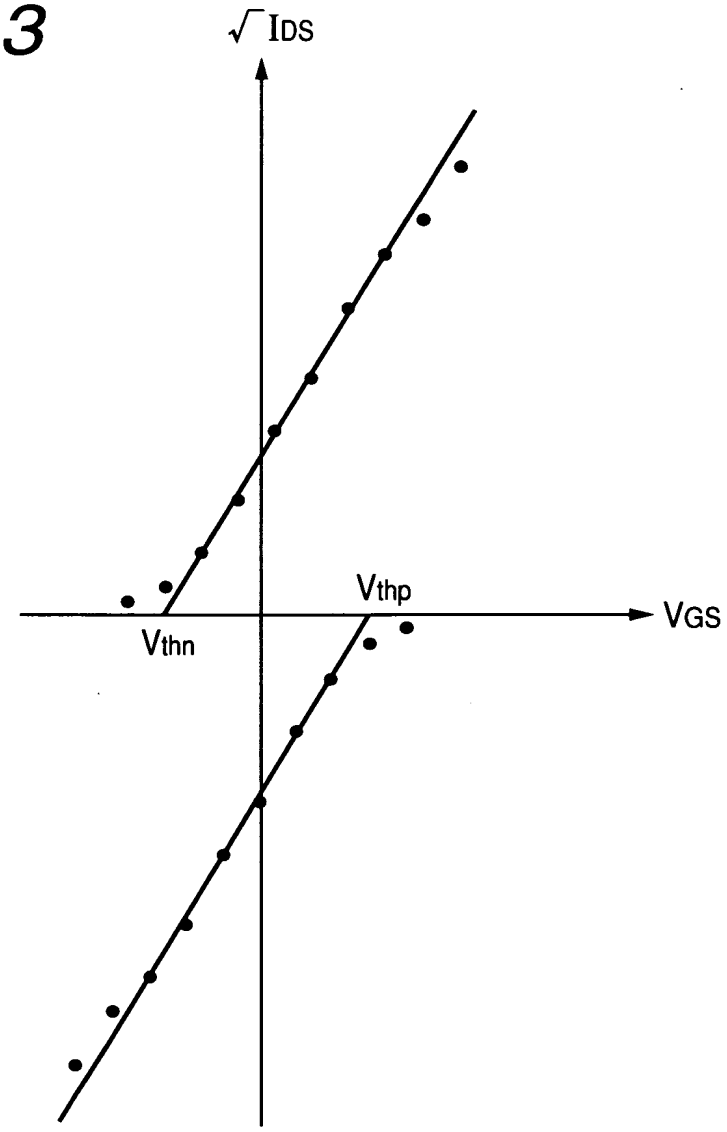

FIG. 4

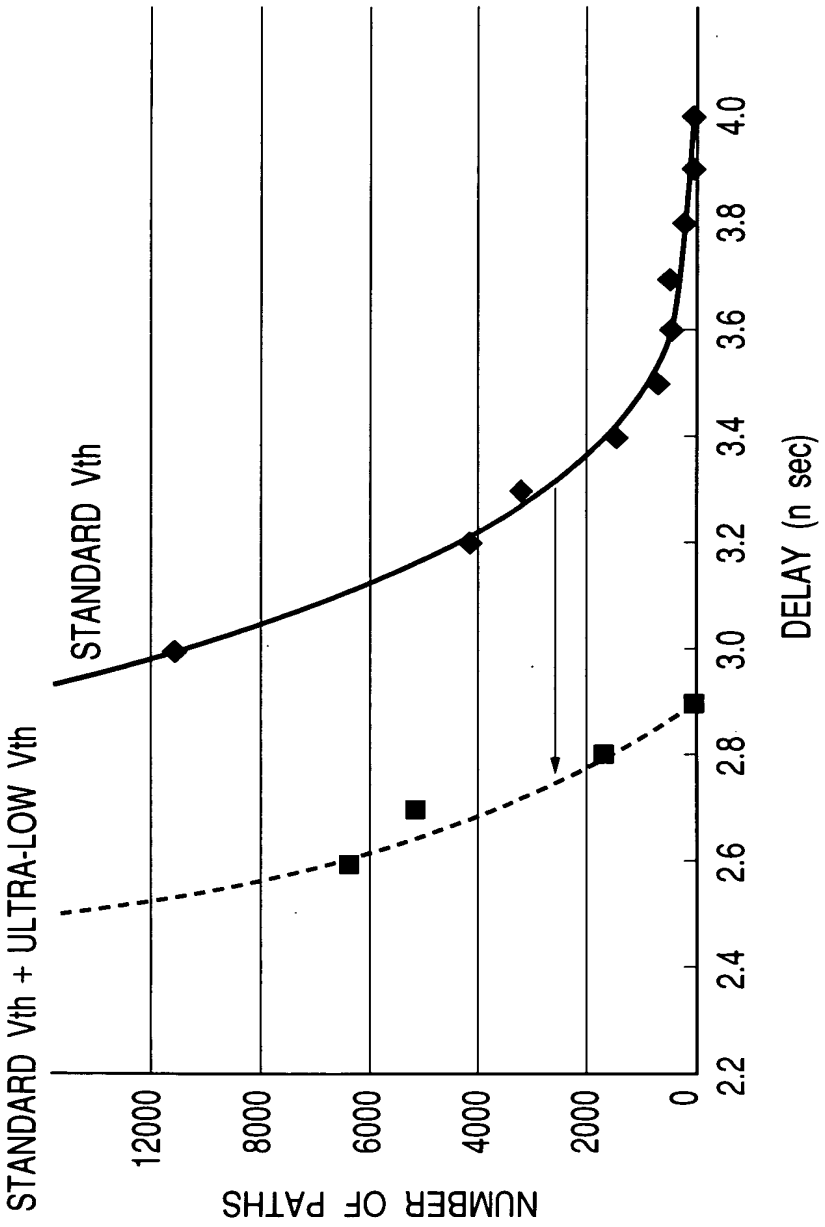
STANDARD Vth
STANDARD Vth + ULTRA-LOW Vth
NUMBER OF PATHS
12000
8000
6000
4000
2000
0
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
DELAY (n sec)

FIG. 5

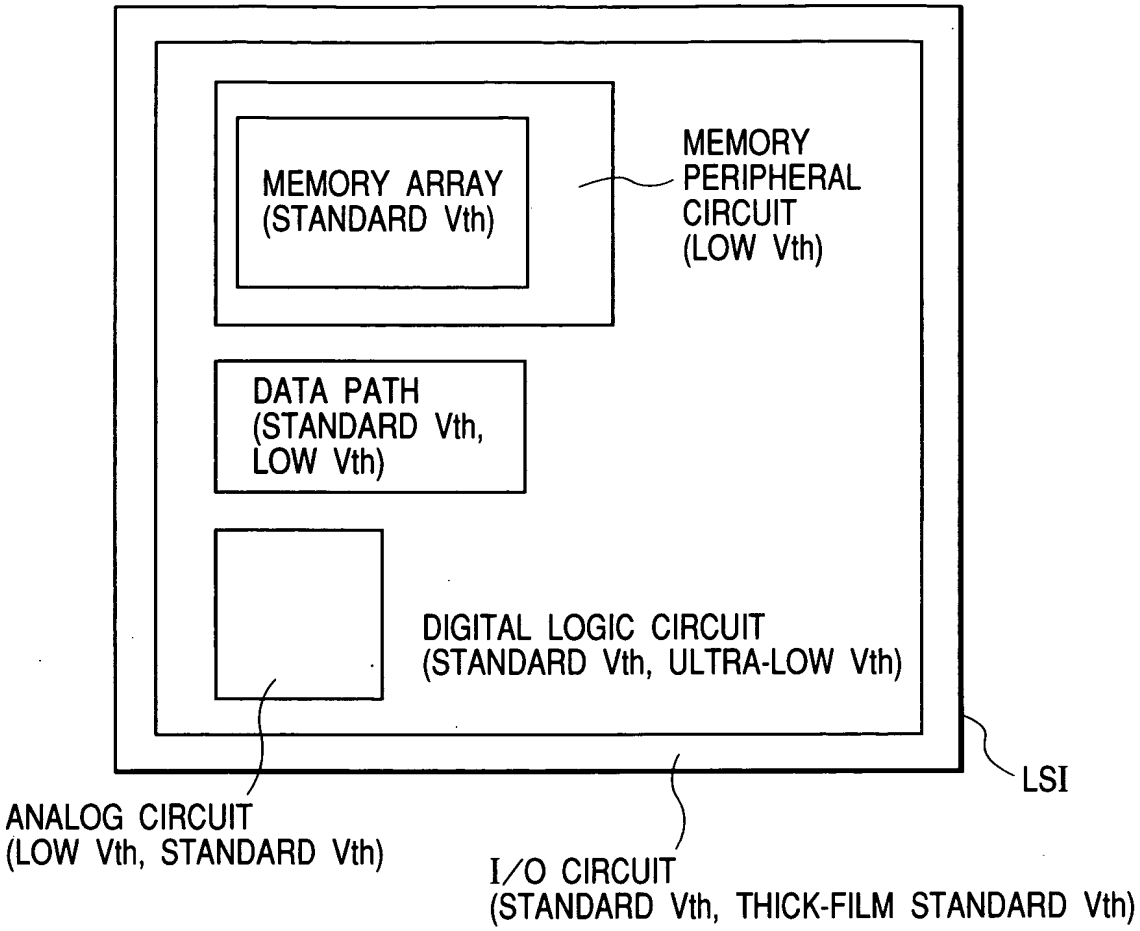
MEMORY ARRAY
(STANDARD Vth)
MEMORY
PERIPHERAL
CIRCUIT
(LOW Vth)
DATA PATH
(STANDARD Vth,
LOW Vth)
DIGITAL LOGIC CIRCUIT
(STANDARD Vth, ULTRA-LOW Vth)
LSI
ANALOG CIRCUIT
(LOW Vth, STANDARD Vth)
I/O CIRCUIT
(STANDARD Vth, THICK-FILM STANDARD Vth)

FIG. 6

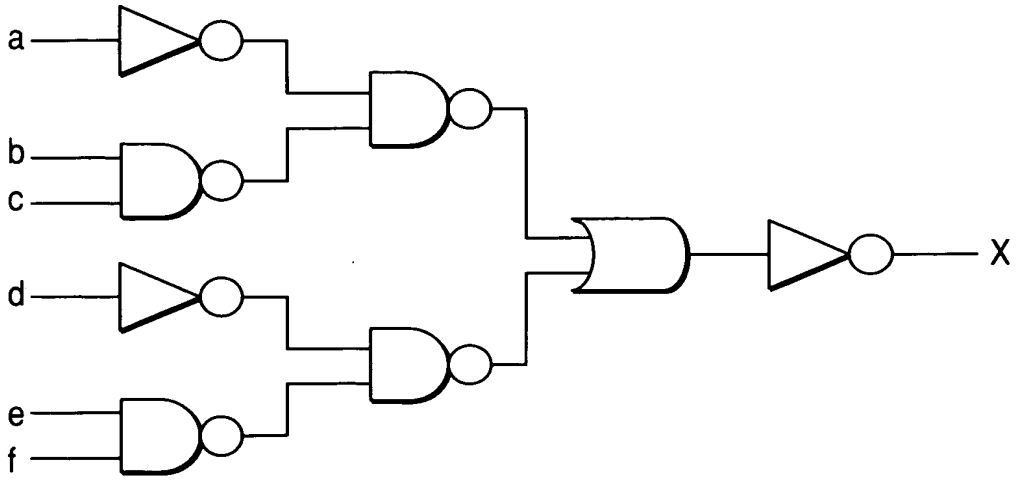
a
b
c
d
e
f
X

FIG. 7

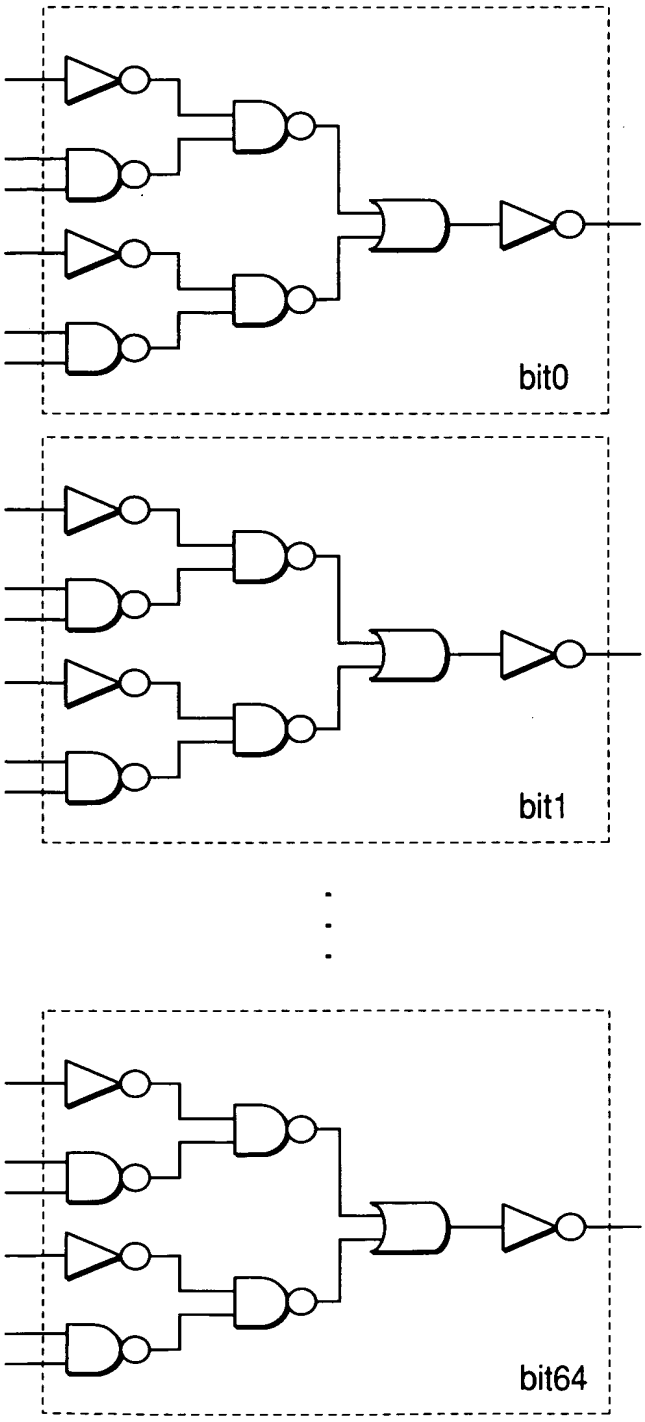

FIG. 8

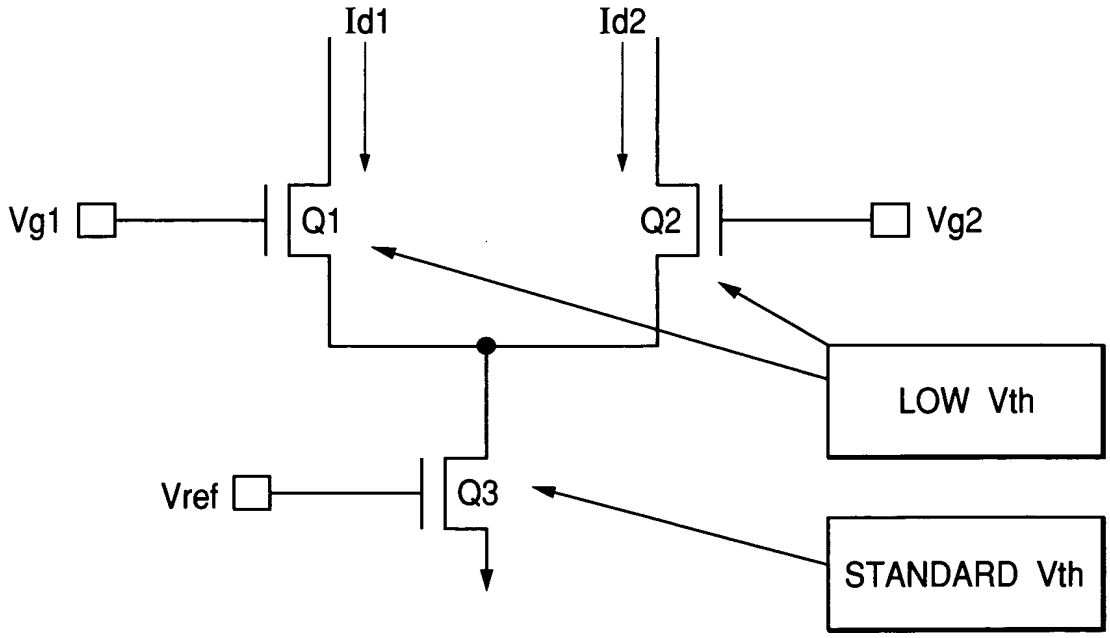

FIG. 9

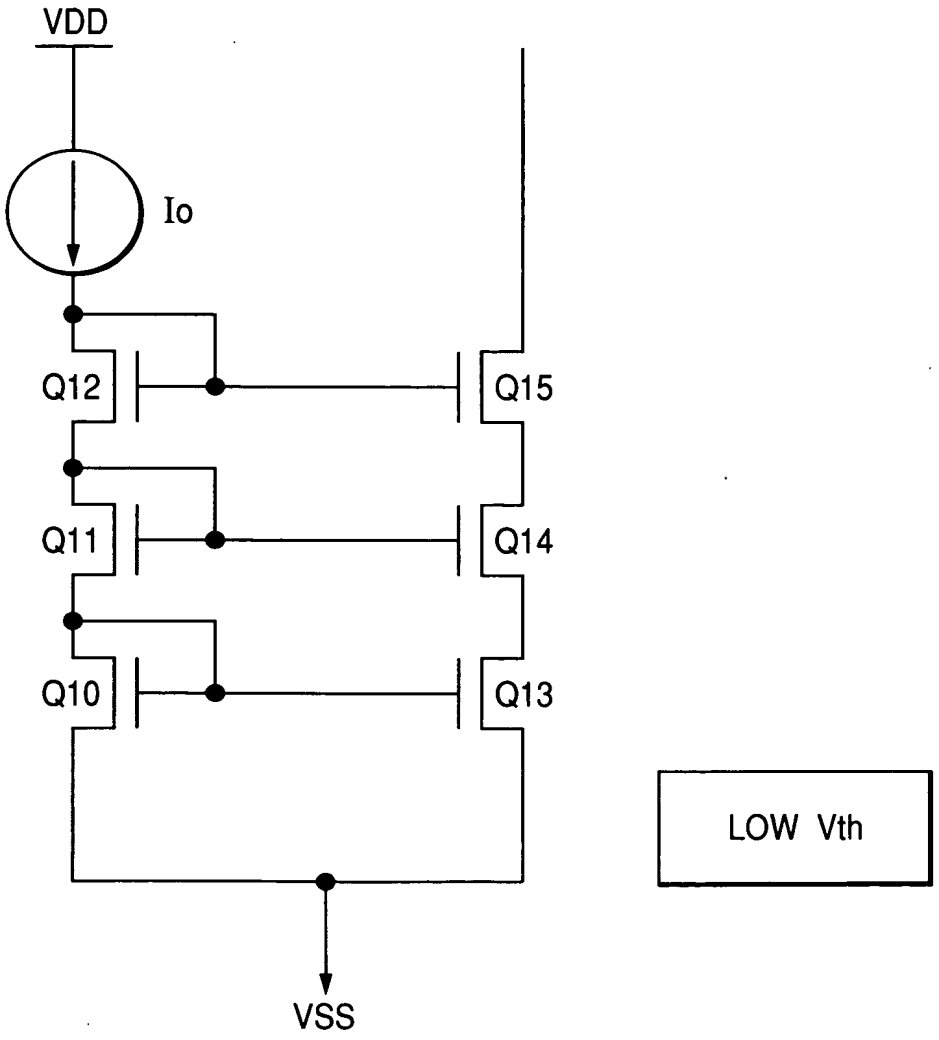

FIG. 10

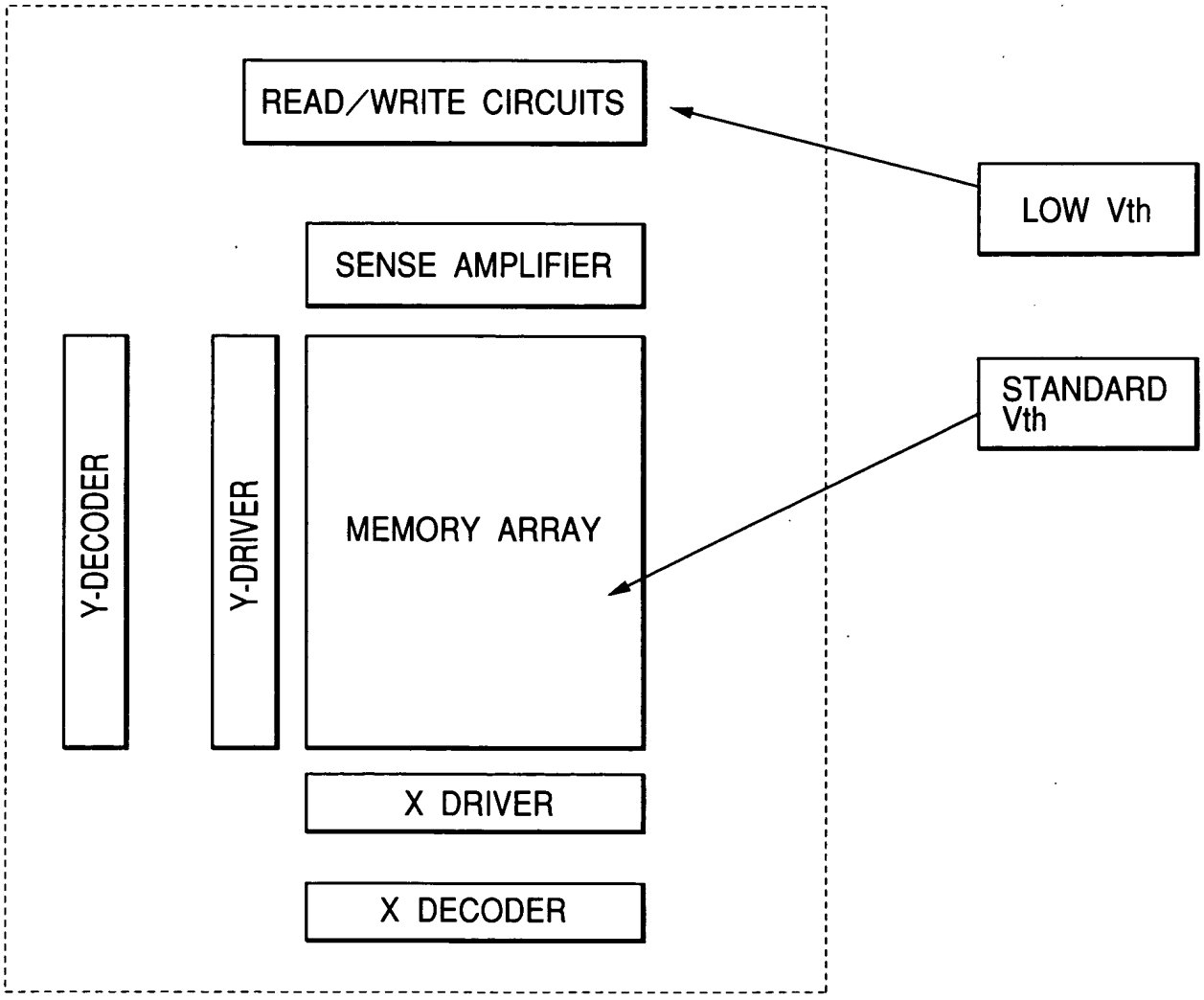
READ/WRITE CIRCUITS
LOW Vth
SENSE AMPLIFIER
STANDARD Vth
Y-DECODER
Y-DRIVER
MEMORY ARRAY
X DRIVER
X DECODER

FIG. 11

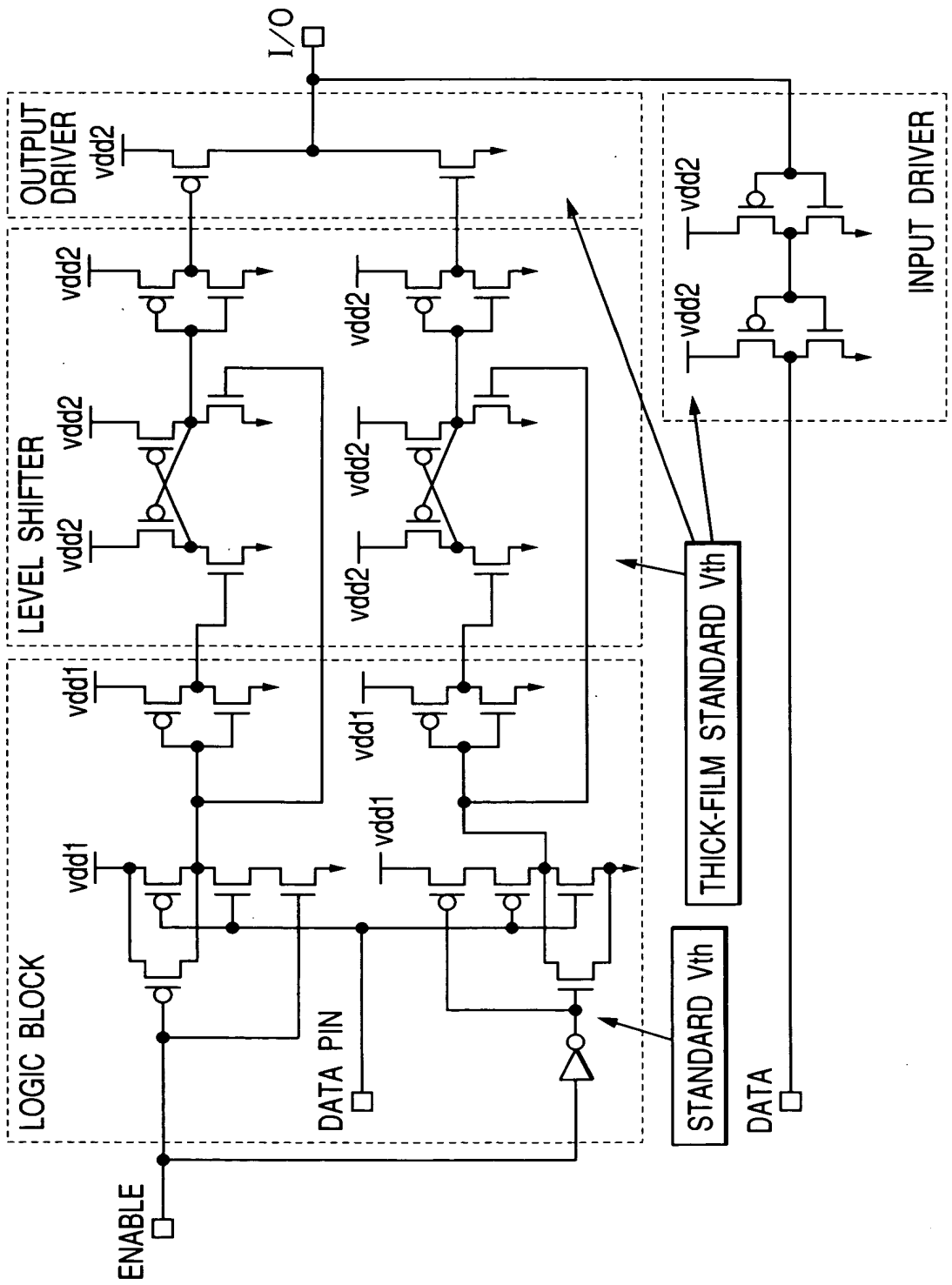
I/O
OUTPUT DRIVER
vdd2
LEVEL SHIFTER
vdd2
vdd1
LOGIC BLOCK
ENABLE
DATA PIN
STANDARD Vth
THICK-FILM STANDARD Vth
DATA
INPUT DRIVER

FIG. 12

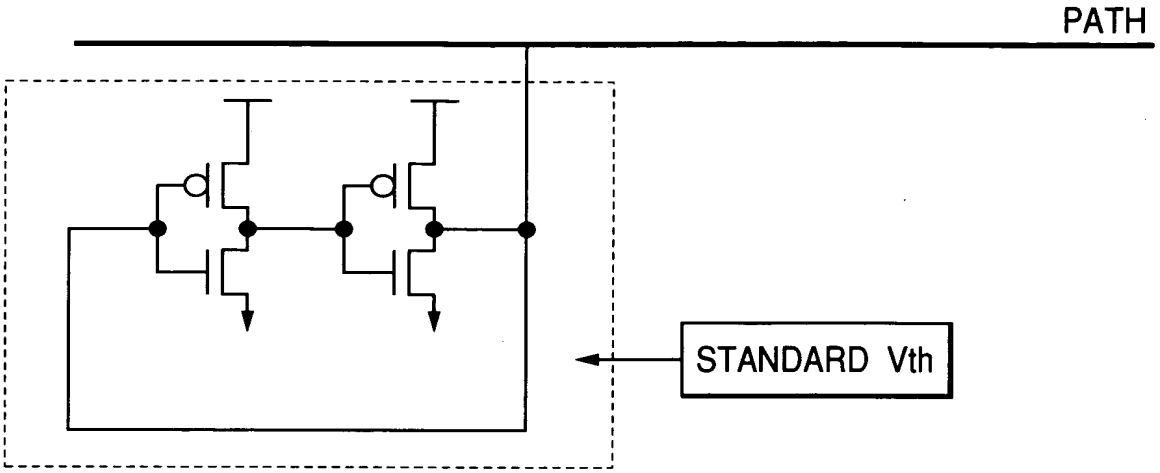
PATH
STANDARD Vth

FIG. 13

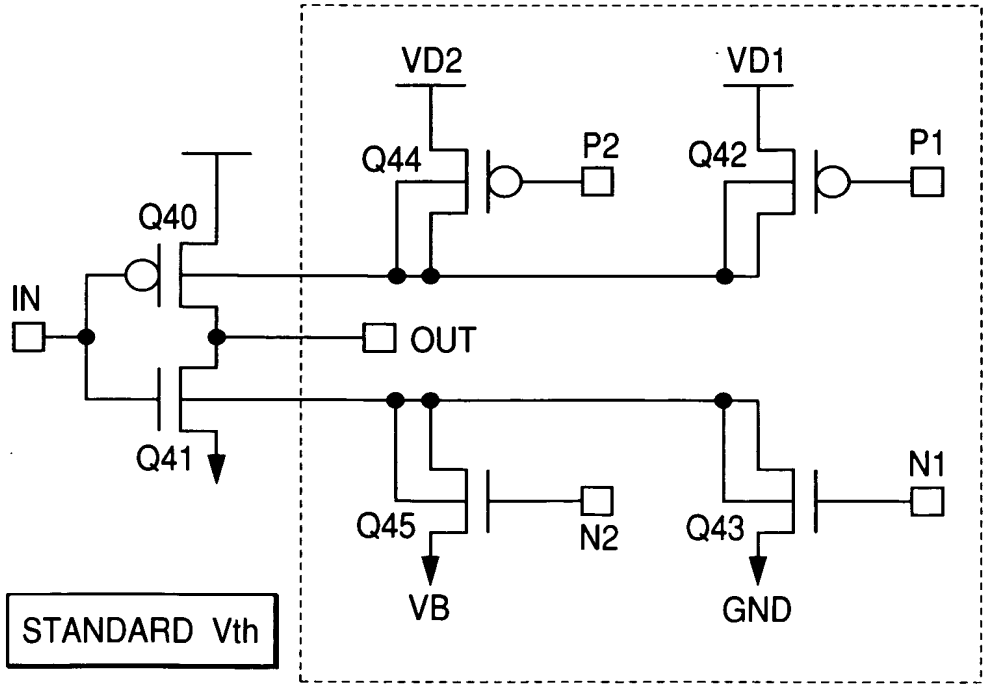
VD2
VD1
Q44
P2
Q42
P1
Q40
IN
OUT
Q41
Q45
N2
Q43
N1
VB
GND
STANDARD Vth

FIG. 14

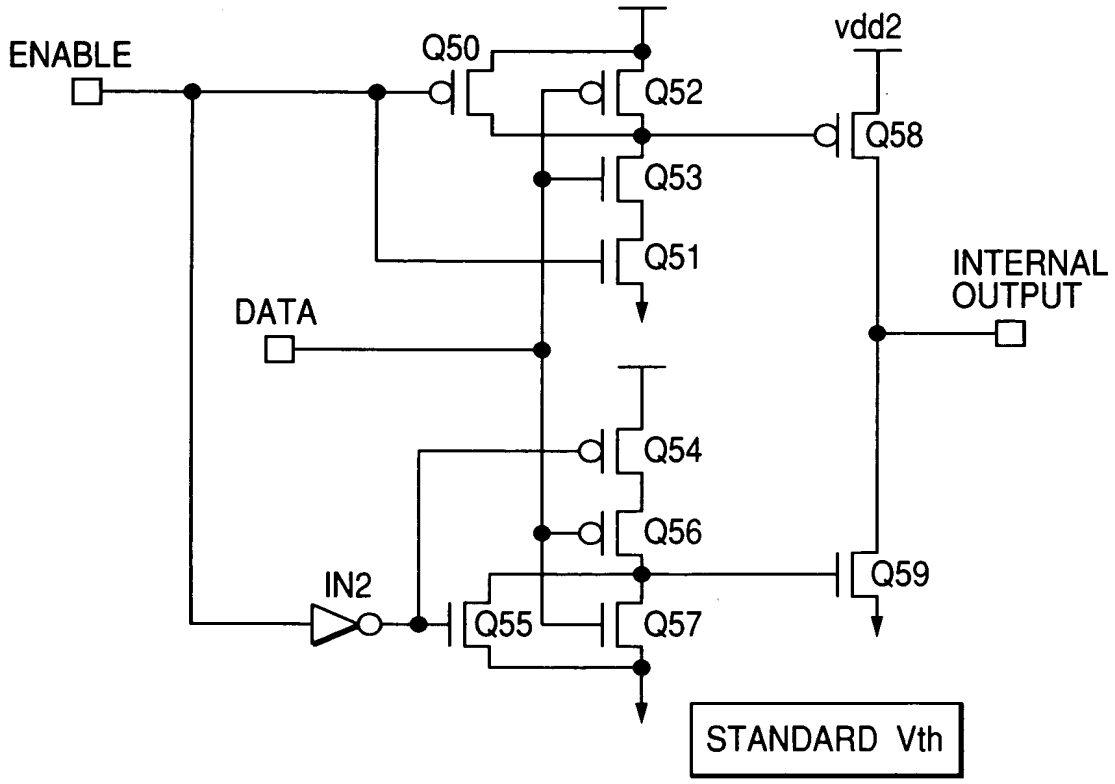
ENABLE
Q50
vdd2
Q52
Q58
Q53
Q51
INTERNAL
OUTPUT
DATA
Q54
Q56
Q59
IN2
Q55
Q57
STANDARD Vth

FIG. 15A

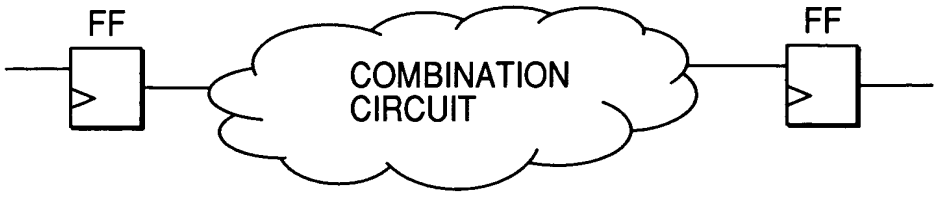

FIG. 15B

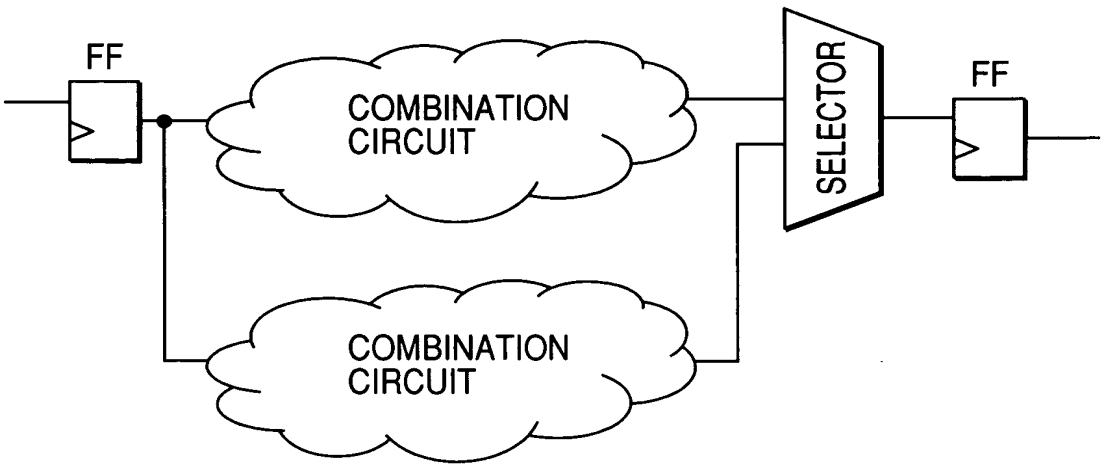

FIG. 16

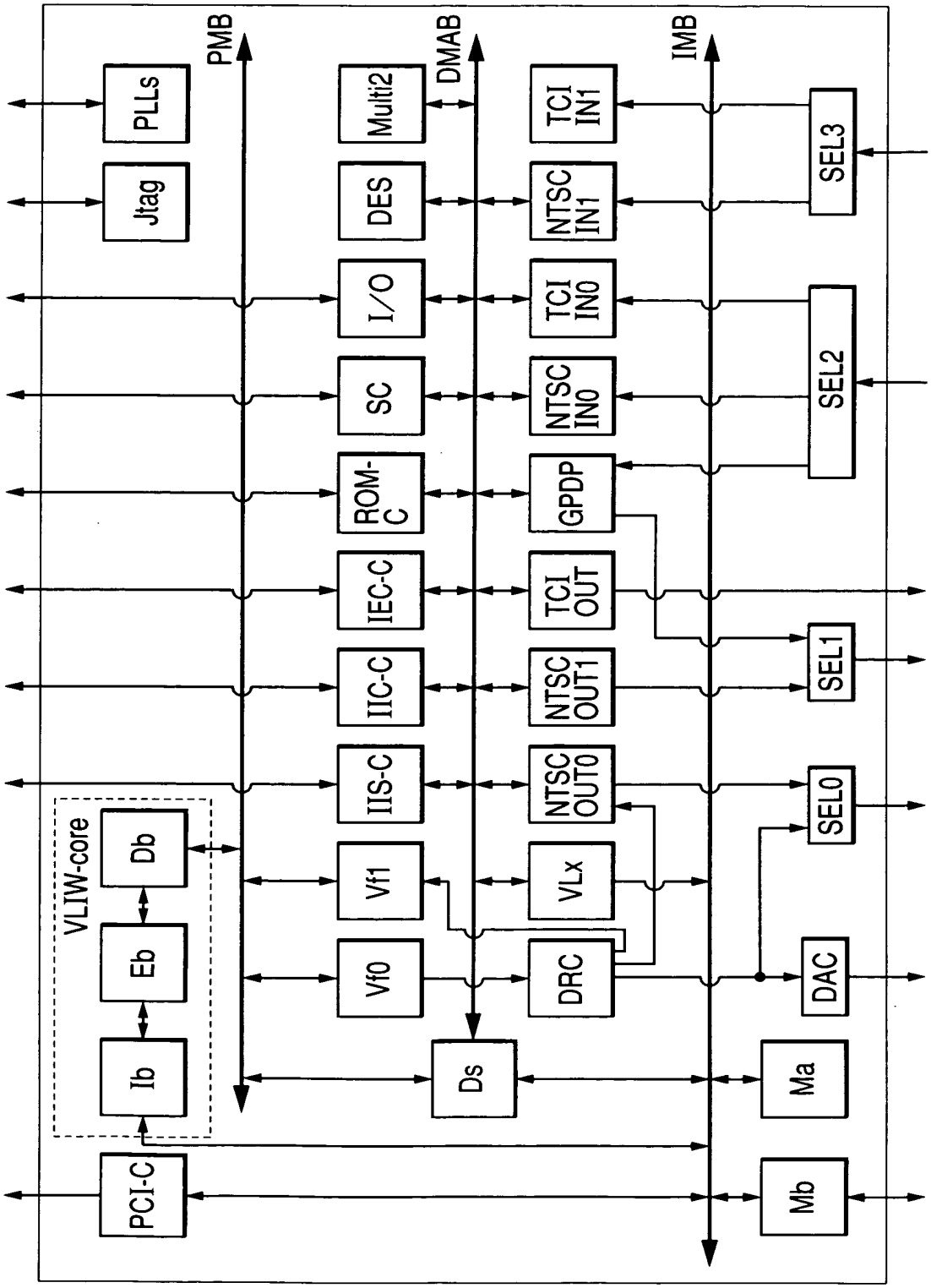
PMB
DMAB
IMB
PLLs
Jtag
Multi2
DES
I/O
SC
ROM-C
IEC-C
IIC-C
IIS-C
Vf1
Vf0
TCI IN1
NTSC IN1
TCI IN0
NTSC IN0
GPDP
TCI OUT
NTSC OUT1
NTSC OUT0
VLx
DRC
SEL3
SEL2
SEL1
SEL0
DAC
VLIW-core
Db
Eb
Ib
PCI-C
Ds
Ma
Mb

FIG. 17

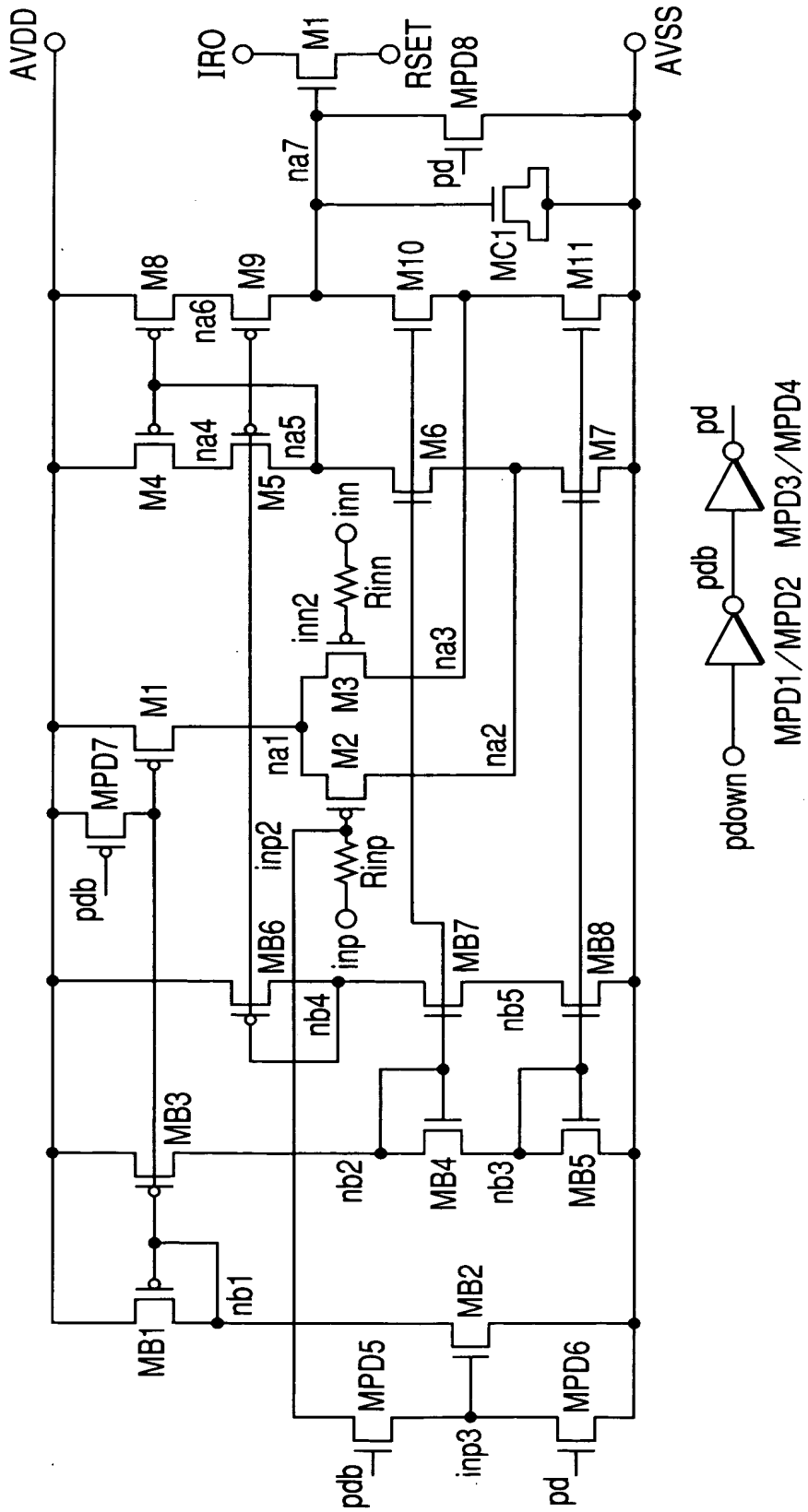
AVDD
IRO
M1
RSET
MPD8
AVSS
na7
pd
MC1
M8
M9
M10
M11
na6
na4
na5
M6
M7
M4
M5
inn
Rinn
inn2
M3
na3
M1
MPD7
M2
na1
na2
pdb
inp2
Rinp
inp
MB6
MB7
MB8
nb4
nb5
MB3
nb2
MB4
nb3
MB5
nb1
MB2
MB1
MPD5
MPD6
pdb
inp3
pd
pd
pdb
MPD3/MPD4
MPD1/MPD2
pdown

FIG. 18